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REPLY UNDER 37 C.F.R. § 1.116 EXPEDITED PROCEDURE EXAMINING GROUP 2116

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:

10/084,566

Filed:

February 27, 2002

Inventor(s):

Madrid, et al.

Title:

A METHOD AND

MECHANISM FOR

GENERATING A CLOCK

SIGNAL WITH A

RELATIVELY LINEAR

INCREASE OR

DECREASE IN CLOCK

FREQUENCY

Examiner:

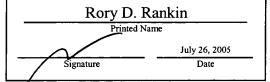
Patel, Nitin C.

Group/Art Unit: 2116

Atty. Dkt. No:

5500-80100

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.



RESPONSE TO FINAL OFFICE ACTION OF MAY 23, 2005

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Mail Stop AF

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Dear Sir:

This paper is submitted in response to the Final Office Action of May 23, 2005, to further highlight why the application is in condition for allowance.

Please amend the case as listed below.